DAΦNE TECHNICAL NOTE

INFN - LNF, Accelerator Division

Frascati, May 20, 1994

Note: **RF-11**

DESIGN AND TEST OF THE CONTROL ELECTRONICS OF THE DAΦNE ACCUMULATOR RF CAVITY

A. Gallo, P. Baldini, R. Boni, F. Lucibello, S. Quaglia

1. Introduction.

The accelerating voltage of the RF cavity of DAΦNE accumulator and main rings require to be low-level controlled in order to set and stabilize all the RF parameters (as accelerating voltage amplitudes and phases, cavity tuning angles, etc.) and to protect the RF transmitter against any dangerous failure. Here we present the design criteria, the architecture and the first test of the low-level analog control of the DAΦNE accumulator cavity RF voltage.

2. Specifications of the analog control electronics.

The most significant RF parameters of the DAΦNE accumulator RF system[1,2] are summarized in Table I.

Table I

RF frequency	73.651 MHz
Harmonic number	8
Number of bunches	1
Max beam current	140 mA
Radiation losses/turn	5.2 KeV
Parasitic losses/turn	1.7 KeV
Number of cavities	1
RF power source	35 kW Tetrode
Max accelerating voltage	200 kV
Cavity shunt impedance	~1.5 MΩ
Max cavity wall losses	13.5 kW
Unloaded cavity Q	~20.000
Loaded cavity Q	~10.000
Cavity half bandwidth	3.7 KHz
Synchrotron frequency	37.76 KHz (@ 200 kV)

The block diagram of the DAΦNE accumulator cavity analog control electronics is shown in Fig. 1. The principal tasks of this system are:

- Switch the cavity "on" and "off";
- Protect the RF system against failures;
- Keep the cavity tuned at a pre-set angle;
- Set and keep the RF voltage phase stable;
- Set and keep the RF voltage amplitude stable;
- Damp the beam center-of-mass instability.

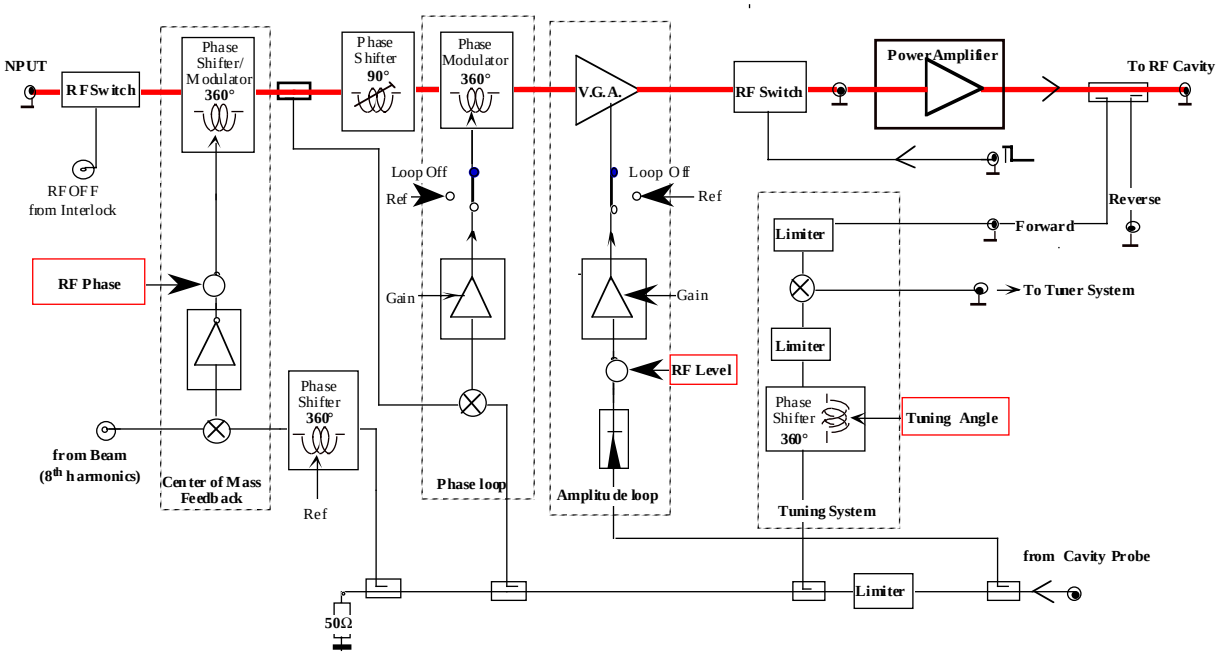

Fig. 1: Accumulator RF control electronics block diagram.

As a general architecture philosophy, the whole low-level equipment shown in Fig. 1 will be based on monolithic devices connected together on a single control board by 50 Ω striplines. This choice was aimed to increase the electronics compactness and reliability. The Douglas CAD/CAM Professional System[3] has been used for the board layout design.

For every specific function various RF devices have been considered and the final choices have been made after severe comparison and experimental tests. Particular attention was paid to the linearity of the phase and amplitude modulators for the RF voltage stabilization in order to make the loop gains independent from the modulator working points.

A complete prototype of the DAΦNE accumulator cavity control electronics based on connectorized modules has been assembled and long time tested on the accumulator cavity prototype. The tests have been satisfactory and the experimental results are reported.

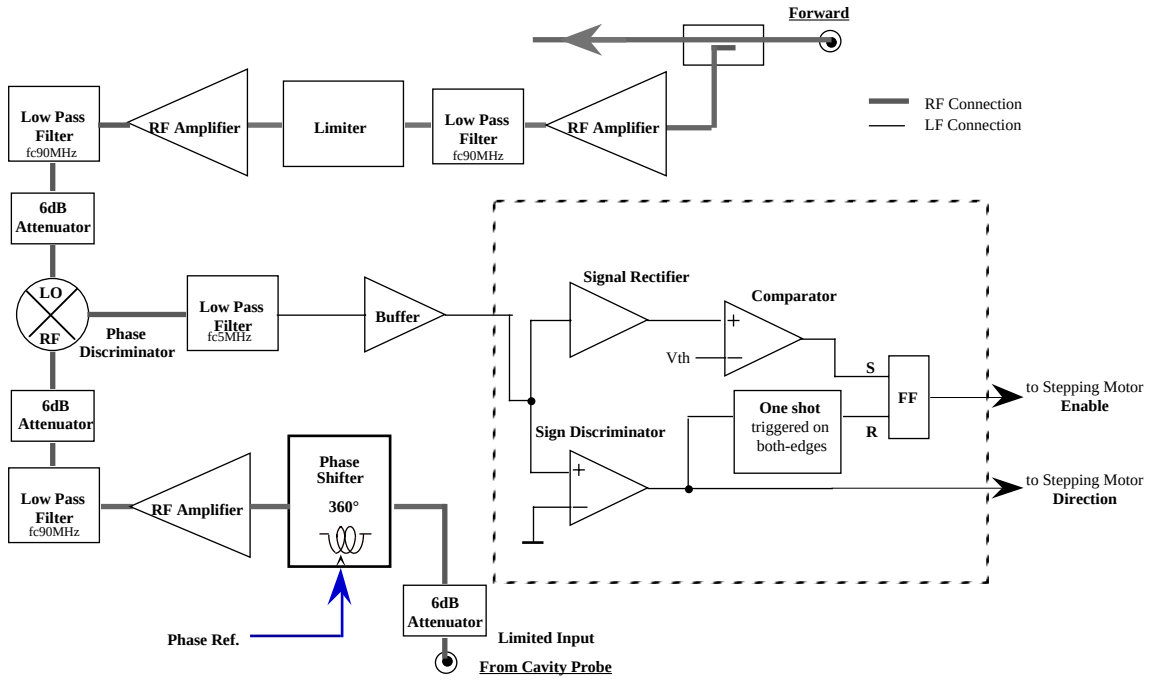

Fig. 2: Tuning System block diagram.

3. The accumulator cavity tuning system.

The block diagram of the accumulator cavity tuning system is shown in Fig. 1 and, in more detail, in Fig. 2. The RF cavity phase is locked to a sample of the forward voltage from the cavity input coaxial line. If a drift of the cavity resonant frequency is large enough to let the phase detector output exceed a given error threshold, a pulse train is fed to the stepping motor which drives the tuning plunger. The pulse train stops when the phase detector output is brought back to zero. A tuning angle different from zero can be chosen by acting on the phase shifter placed behind the phase detector RF input. This control allows to add Robinson damping to the accumulator RF system.

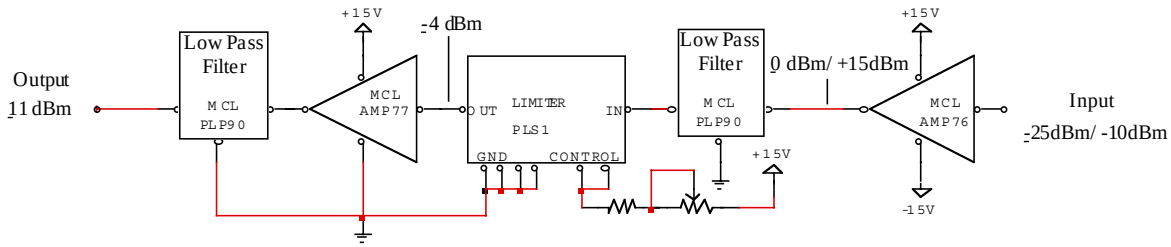

Fig. 3a: Limiter schematic circuit.

Since the phase detector sensitivity strongly depends on the RF signal levels, the tuning system requires efficient limiters to feed the detector at constant levels independently from the accelerating voltage amplitude.

While keeping their output level constant in spite of input variations, the limiters should also not introduce a too large phase drift that would produce unwanted reactions of the tuning system. Two balanced limiter circuits have been especially developed for this task; the circuit schematics is shown in Fig. 3a, while a measure of the amplitude and phase drift of the two circuits for an input level variation of 15 dB is shown in Fig. 3b and 3c.

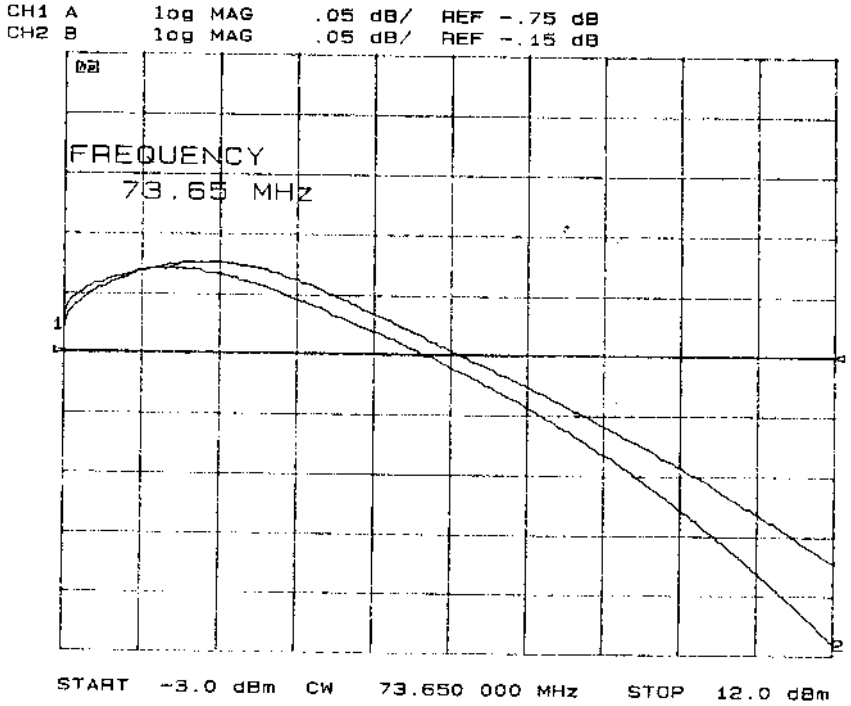

Fig. 3b: Limiter output level variation.

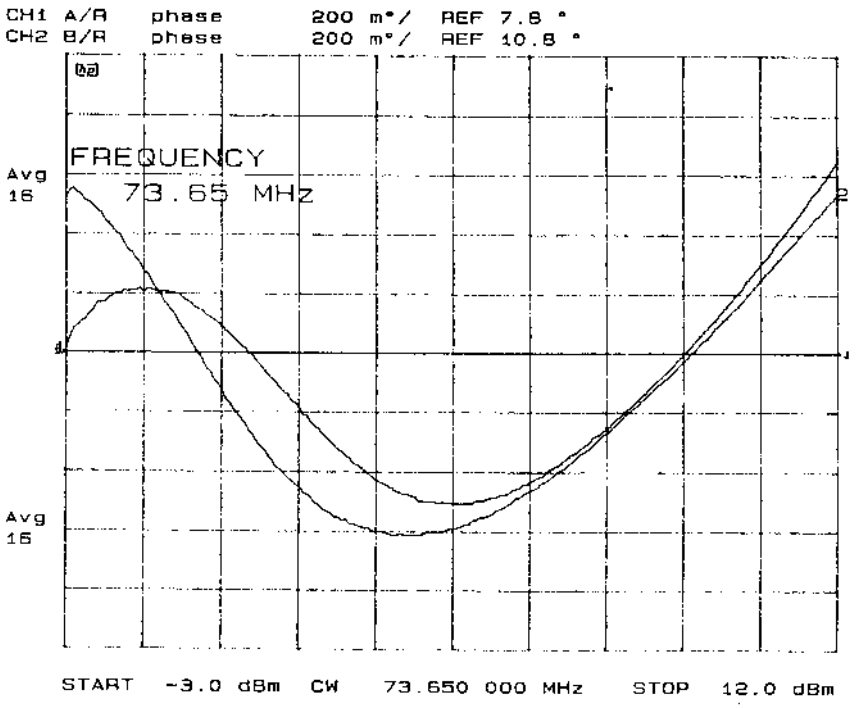

Fig. 3c: Limiter output phase variation.

The total output amplitude and phase variations are within 0.35 dB and 1.3° respectively. The response of the phase detector with the two RF limiters at inputs is shown in Fig. 4. The slope of the curve (i.e. the detector sensitivity) is almost constant in a wide range around the zero and, due to the presence of the limiters, is practically independent from the RF input level.

The tuning system performed satisfactorily and reliably during a 4 week test of the control electronics prototype. The experimental test has also shown that a tuning angle accuracy of about 2° is compatible with stable tuning system operation.

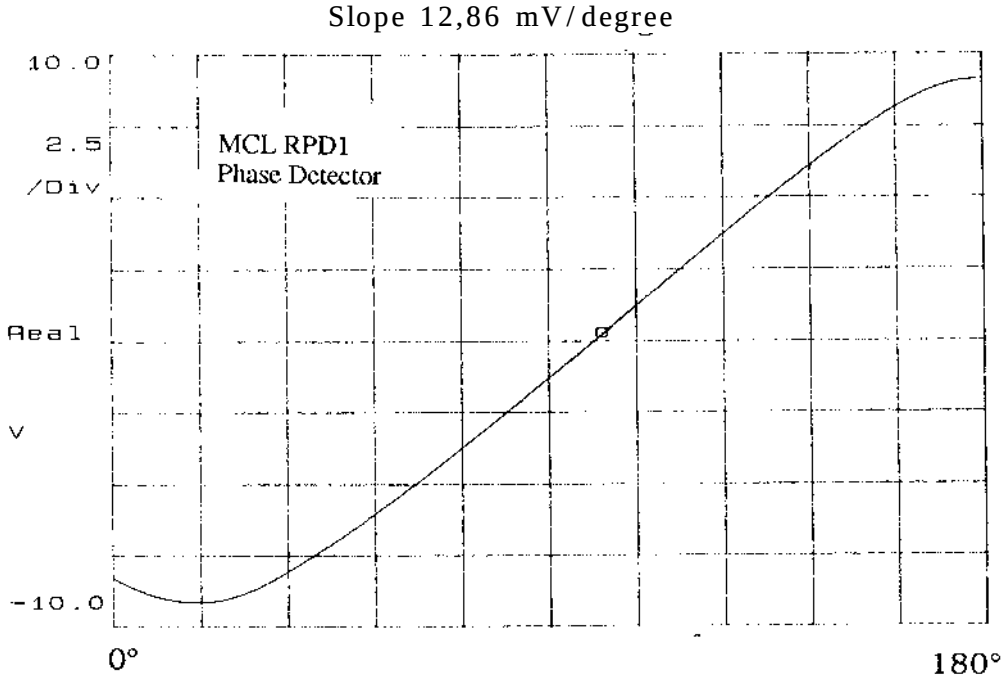

Fig. 4: Phase detector characteristics.

4. The phase stabilization loop.

The phase of the accumulator cavity accelerating voltage has to be locked to the DAΦNE timing system that synchronizes the operation of the various machine components. Therefore, as shown in Fig. 5, a sample of the accelerating voltage is locked to a 73.65 MHz RF master signal coming from the timing system. Any phase drift from equilibrium is detected by a mixer of the same kind of that used in the tuning system, and corrected by a phase modulator through an error amplifier.

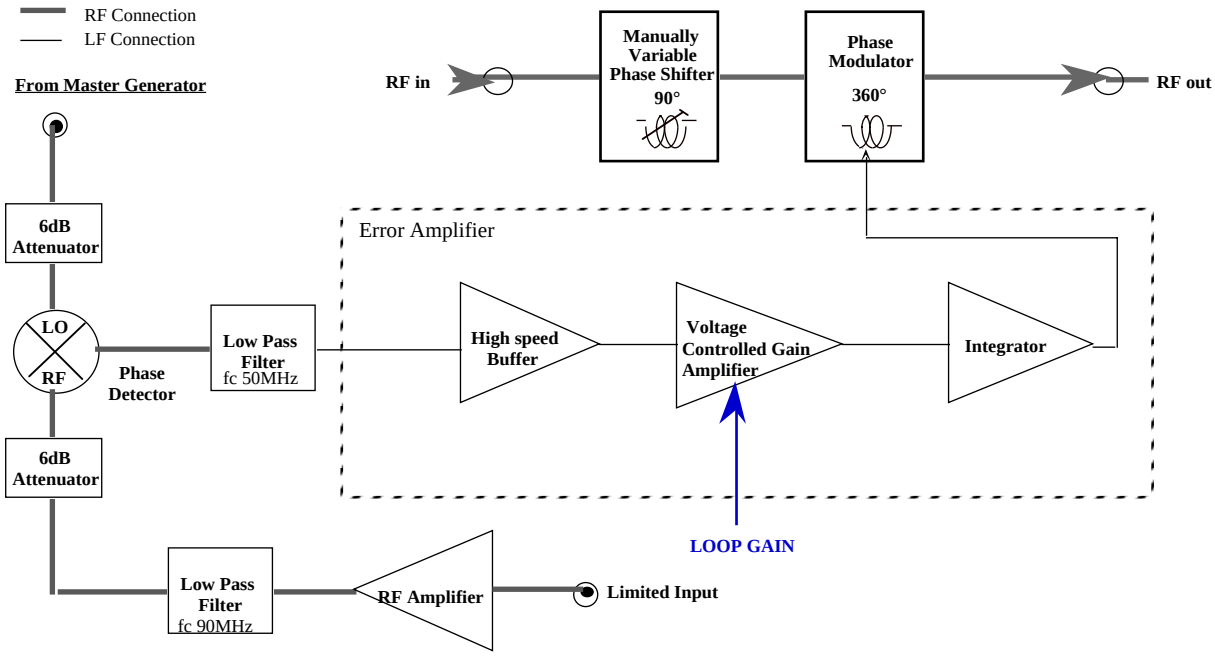

Fig. 5: Phase Loop block diagram.

The phase modulator characteristics is shown in Fig. 6. The phase curve is linear all over the 360° wide dynamic range.

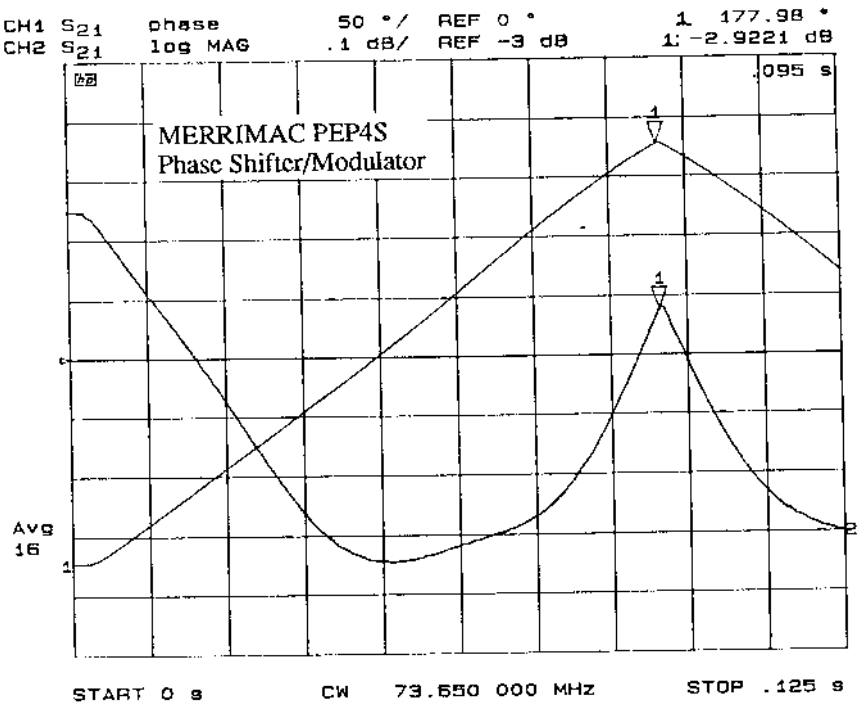

Fig. 6: Phase modulator characteristics
(measured with 8 Vpp triangular wave at control input).

The error amplifier is a three stage channel based on high-speed OP AMPs[4] to increase the bandwidth of the loop. The first stage is a high-speed buffer which takes the error signal from the phase detector. The second stage is a variable gain amplifier controlled by an external analog voltage that allows to set and change the loop gain through the machine Central System. The third stage is an integrator that also compensates the cavity bandwidth with a zero-pole cancellation. The open-loop response of the whole phase stabilization system, including the delay of a 100 m coaxial cable, has been obtained from closed loop measurements[5] and it is shown in Fig. 7. Once the cavity response has been compensated, a loop bandwidth larger than 100 KHz can be obtained, with a gain exceeding 70 dB at 50 Hz and 55 dB at 300 Hz.

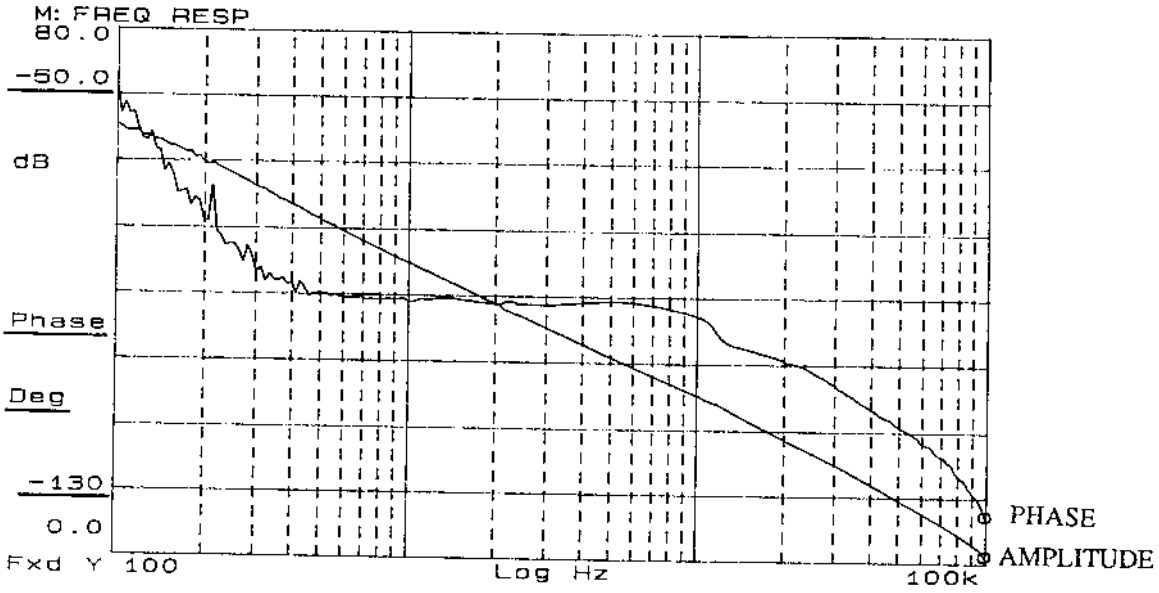

Fig. 7: Open loop transfer function of the phase stabilization system.

5. The amplitude stabilization loop.

The accelerating voltage amplitude stabilization is required to cut the residual amplitude modulation coming mostly from ripple of the high voltage supply of the RF power amplifier that feeds the cavity. The detailed block diagram of that loop is shown in Fig. 8. The amplitude of the accelerating voltage, sampled with a peak detector, is compared with a variable dc reference and the error signal drives an amplitude modulator through an error amplifier very similar to that described in the previous paragraph.

The amplitude modulator is a voltage controlled gain amplifier; it is a monolithic chip based on fast, wideband current feedback OP AMPs[4] whose characteristics, measured at 73.65 MHz, is shown in Fig. 9.

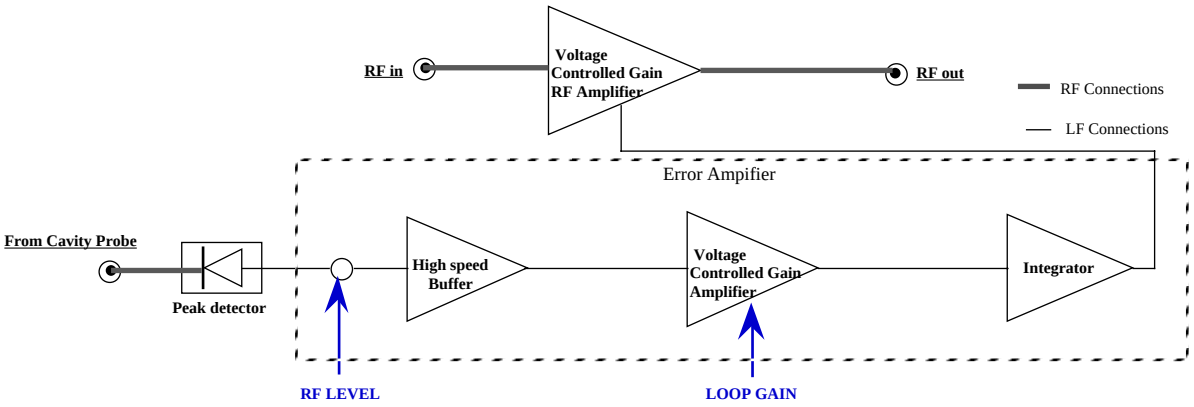

Fig. 8: Amplitude Loop block diagram.

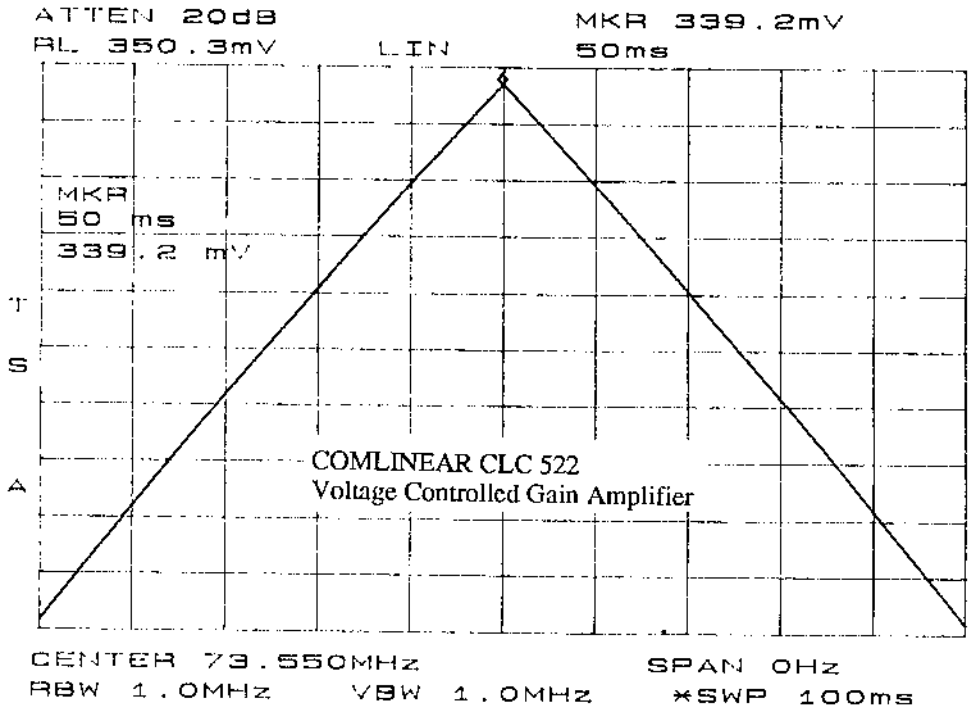

Fig. 9: Amplitude modulator characteristics
(measured with 2 Vpp triangular wave at control input).

Differently from other conventional RF amplitude modulators, this device has a very good linearity in a dynamic range larger than 40 dB; therefore the amplitude loop total gain is independent on the modulator working point. The experimental open-loop response of the whole amplitude stabilization system, including the delay of a 100 m coaxial cable, is shown in Fig. 10. Like for the phase loop, once the cavity response has been compensated by the error amplifier end stage, a loop bandwidth larger than 100 KHz can be obtained, with a gain exceeding 70 dB at 50 Hz and 55 dB at 300 Hz.

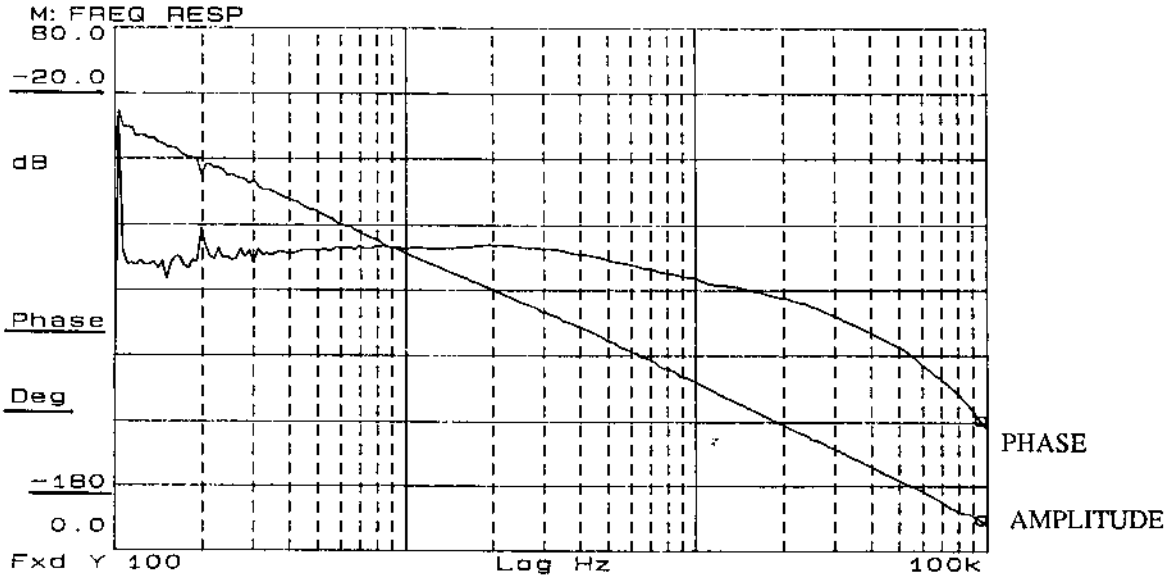

Fig. 10: Open loop transfer function of the amplitude stabilization system.

6. The center-of-mass feedback.

In some operating conditions the beam-cavity interaction can produce an antidamping term in the synchrotron equation leading to beam center-of-mass instability. To cure this effect an extra damping term must be introduced. This can be obtained by giving to the beam an additional energy kick proportional to the time derivative of the instantaneous deviation from the synchronous phase. The block diagram of the low level electronics dedicated to this feedback is shown in Fig. 11.

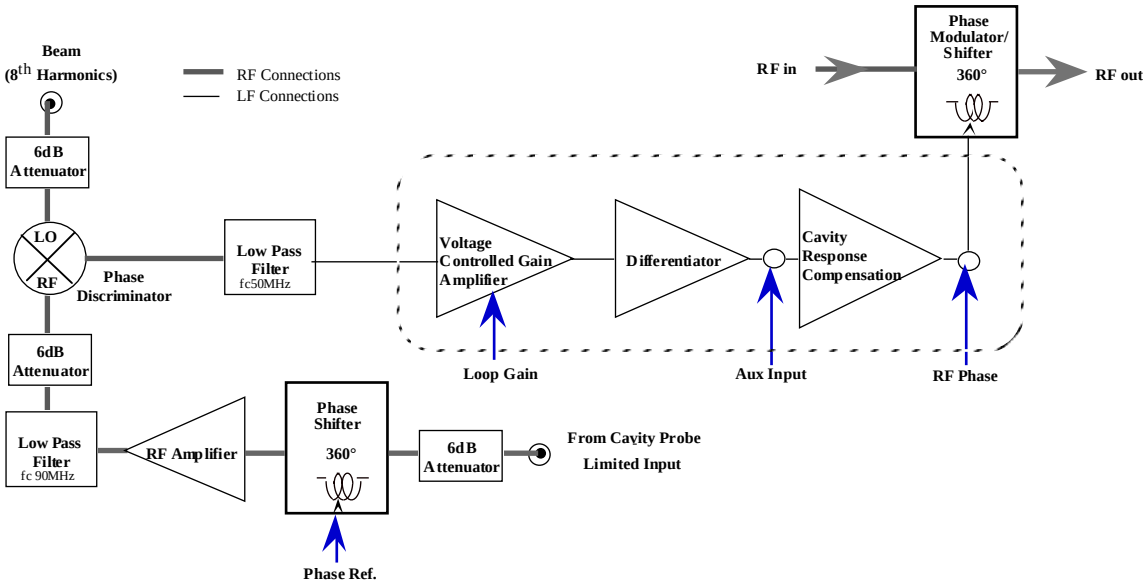

Fig. 11: Center-of-mass feedback block diagram.

A phase detector discriminates the phase of the 8th beam harmonic with respect to the cavity voltage, while the following three amplification stages provide loop gain adjustment, time domain signal differentiation and cavity frequency response compensation respectively. This last function is required since the DAΦNE accumulator synchrotron frequency is larger than the cavity bandwidth and any modulation of the RF incident power at the synchrotron frequency is cut by the cavity response. An auxiliary input port is available to excite the beam for beam transfer function measurements.

Since the differentiator is an AC circuit, the feedback signal at phase modulator control port has no DC components. By adding a DC voltage to the feedback signal the phase modulator can be used also as a phase shifter to adjust the phase of the accumulator accelerating voltage according to machine timing requirements.

The frequency response of the three stage amplifier is shown in Fig. 12. Each stage is based on fast current feedback OP AMPs and the voltage controlled amplifier stage gives a 60 dB loop gain dynamic range. The differentiator stage gives the initial +20 dB/decade slope while the cavity response compensation brings the final slope of the circuit frequency response up to +40 dB/decade. It is interesting to remark that a similar frequency response can be hardly obtained with voltage feedback OP AMPs which, unlike current feedback devices[4,6,7], are intrinsically unstable when connected as differentiators.

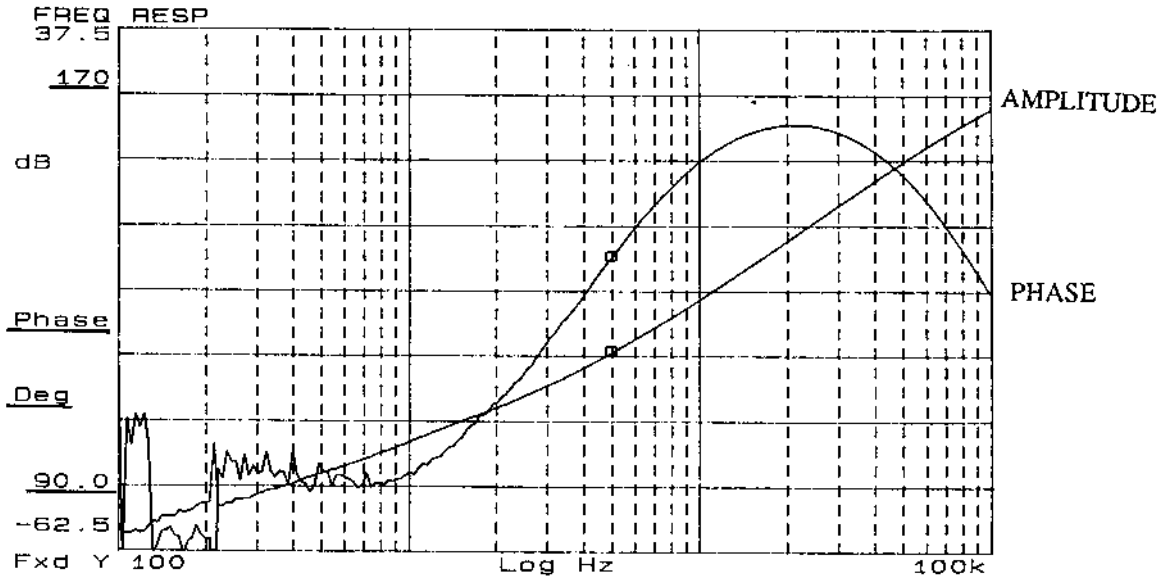

Fig. 12: Frequency response of the center-of-mass feedback LF Amplifier.

7. RF switch on procedure, interlock system, computer interface.

In the control board RF line, as shown in Fig. 1, there are two TTL driven, fast RF switches to pulse the RF power in the switch-on procedure and to switch-off the power in case of failure detected by the interlock system.

During the switch-on procedure, the RF pulsed operation is preferred since it allows to find the right cavity tune at a considerably lower average power level. The procedure is therefore safe even if the cavity is initially completely mismatched and all the forward power is reflected. Moreover, the pulsed operation is suitable for the cavity vacuum conditioning.

The interlock signals that control the other switch come either from a dedicated PLC or, in some special cases, directly from the front end sensors (for instance, the alarm signal from the arc detector of the high power ferrite circulator interposed between the tetrode amplifier and the cavity).

The Telemecanique TSX P47425 PLC has been used to manage the interlocks of all the RF system parameters including those related to the high power circulator, cooling and vacuum systems. If necessary, other fast external interlocks can be connected to the control board through some extra RF disable input ports.

A VME crate equipped with DAC, ADC and I/O boards will be the interface between the RF control board and the central computer control system. The control architecture is such that all the RF system parameters will be available directly at the operator level[8].

In order to preserve a tolerable signal-to-noise ratio, all the signals coming to the control board from the VME crate are carefully filtered.

8. Conclusion.

An analog electronic board for the complete low-level control of the DAΦNE accumulator RF system has been fully designed. A control electronics prototype based on connectorized devices has been assembled and long time tested. The test results are considered fully satisfactory since the various control sections perform reliably and meet the specifications. Particularly, the measured performances of the amplitude and phase loop in terms of gain and bandwidth are remarkable. A first complete board should be ready for experimental test in July '95. The design of the electronic boards for the low-level control of the DAΦNE main ring RF systems, based on the same architecture, is well in progress.

Acknowledgments

We would like to thank A. Cecchinelli, M. Scampati and A. Sprecacenere for their collaboration to the design, hardware assembling and experimental tests described in this report.

We also appreciated very much the helpful and clarifying discussions with Dr. M. Serio.

References

[1] R. Boni et al., *The DAΦNE RF System Parameters*, DAΦNE Technical Note RF-3 (1991).

[2] S. Bartalucci et al., *RF Cavity Design for the DAΦNE Accumulator*, DAΦNE Technical Note RF-4 (1991).

[3] *The Douglas CAD/CAM Professional System*, Douglas Electronics inc., 718 Marina Boulevard, San Leandro, CA 94577 U.S.A.

[4] *Solutions with speed*, 1993/94 Databook, Comlinear Corporation 4800 Wheaton Drive, Fort Collins, CO 80525 U.S.A.

[5] A. Ceccarelli et al., INFN LNF Accelerator Division internal report RF66 (1990), in Italian.

[6] J. Millman, *Microelectronics*, Mc Graw-Hill inc. (1979).

[7] Gray-Mayer, *Analysis and Design of Analog Integrated Circuits*, Wiley.

[8] B. Caccia et al., *The DANTE Control System* INFN LNF internal report LNF-92/054 (1992).