DAΦNE TECHNICAL NOTE

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Note: **CD-8**

DAΦNE TIMING STATES UPDATE

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The first two sections of this note present the updated list and description of the DAΦNE timing states. The third section describes the relevant features of the electronic module that distributes the timing information all along the facility. The note replaces the previous CD-4.

1. General Rules

Table 1. DAΦNE Timing State Tokens

TOKEN	NAME	FAMILY
LTO	LINAC Triggers OFF	LINAC
LSB	LINAC Stand By	LINAC
LSP	Beam from LINAC to Spectrometer	LINAC
LBT	Beam from LINAC to BTF	LINAC
LAC	Beam from LINAC to Accumulator Ring	LINAC
AEX	Accumulator Extraction	Accumulator Ring
AMR	Accumulator Extraction & Main Rings Injection	Accumulator Ring
VM1	Pulsed Magnet DHPTT01 Pre-Trigger	Various
VM2	Pulsed Magnet DHPTT02 Pre-Trigger	Various
VMS	Pulsed Magnet DHPTS01 Pre-Trigger	Various
VKP	Main Rings Kickers Pre-Triggers	Various
VCA	Calibration State	Various

- Each *state* has 20 ms duration.

- More states can exist simultaneously. However some exclusions apply, see later.

- Each of the 12 states has an associated bit in a *state word*. The latter includes also the particle mode (1 bit) (electrons or positrons), the number of the main ring bucket to be filled (7 bit) and an enable line (1 bit).

- The state words are composed in *state sequences* of arbitrary length that regulate the machine timing.

- A high level program must allow the construction of both state words and state sequences. It must automatically check the incompatibilities and the syntax rules pointed out in this note.

- Three families of states exist: LINAC (the state token first letter is L); ACCUMULATOR RING (letter A); VARIOUS (letter V). States belonging to the same family cannot be simultaneous (this restriction does not apply to the VARIOUS family).

- All the single set of simultaneous states in the state sequence must include a LINAC state.

- The timing system does not control complex sequences such as, for example, DC magnet polarity inversion between positron and electron modes.

2. States Description

1) LINAC TRIGGERS OFF (LTO).

The LINAC needs two different triggers: one for the electron gun cathode grid (**gun trigger**), the other for the system (modulators, PC pulser, etc.) (**system trigger**). In the LTO state no LINAC trigger will be enabled. The minimum repetition rate for the system trigger is 10 Hz, this implies that **no more than 4 (four) consecutive LTO are allowed** in a state sequence.

State Incompatibility: LSB, LSP, LBT, LAC, AEX, AMR.

2) LINAC STAND BY (LSB).

In the LSB state only the system trigger is enabled. This will allow to keep the pulsed systems within temperature with no accelerated beam.

State Incompatibility: LTO, LSP, LBT, LAC, AEX, AMR.

3) BEAM FROM LINAC TO SPECTROMETER (LSP).

The LSP timing state enables both the LINAC triggers and the triggers of the spectrometer branch line. In order to send the beam inside the spectrometer the pulsed magnet DHPTS01 must be on during the LSP state. The power supply of this magnet needs a charging pre-trigger, which is given by t**he timing state VMS** (see dedicated description) that **must precede the LSP state**. **These two states must be separated each other by exactly 23 timing states**. The firing trigger is automatically derived from the pretrigger independently from the timing. The DHPTS01 power supply can operate at 2 Hz maximum rep. rate. **This implies that two consecutive LSP states must be separated each other by at least 24 timing states**.

State Incompatibility: LTO, LSB, LBT, LAC, VMS.

4) BEAM FROM LINAC TO BTF (LBT).

The LBT timing state enables both the LINAC triggers, the trigger for the diagnostics on the BTF line and the possible triggers needed by the external devices in the BTF hall. In order to transport the beam in the BTF it is necessary to turn on a DC dipole magnet. This operation is part of an asynchronous long time machine state sequence that does not interact with the timing system.

State Incompatibility: LTO, LSB, LSP, LAC.

5) BEAM FROM LINAC TO ACCUMULATOR RING (LAC).

The LAC timing state enables both the LINAC triggers and the triggers for the Accumulator injection (kickers, diagnostics, etc.).

State Incompatibility: LTO, LSB, LSP, LBT, AEX, AMR.

6) ACCUMULATOR EXTRACTION (AEX).

The AEX timing state enables the triggers of the Accumulator kickers and of the diagnostics related with the extraction from the Accumulator. It also enables the trigger for the pulsed magnet DHPTT01 power supply for restoring the polarity for the Accumulator injection. Moreover, in order to send the beam towards the Main Rings the pulsed magnet DHPTT02 must be on during the AEX state. The power supply of this magnet needs a charging pre-trigger, which is given by t**he timing state VM2** (see dedicated description) that **must precede the AEX state**. **These two states must be separated each other by exactly 23 timing states**. The firing trigger is automatically derived from the pretrigger independently from the timing. Always for the Accumulator extraction, the power supply of the pulsed magnet DHPTT01 needs a 'pre-trigger' for inverting the polarity. This is done by **the timing state VM1, that must precedes AEX by exactly 5 timing states.** This polarity switching of the pulsed magnet DHPTT01 takes ~ 95 ms, while the pulse duration of the DHPTT02 is ~ 30 ms, this means that in order to prevent inadvertent passage of the beam inside these magnets during these transition phases, **the AEX state, the previous 5 states and the following 5 states are not compatible with the LAC states**.

Moreover, the DHPTT01 and DHPTT02 power supplies operate at 2 Hz maximum rep. rate. **This implies that two consecutive AEX states must be separated each other by at least 24 timing states**. Finally in order to avoid that, during this phase, the extracted beam goes back to the LINAC, the spectrometer magnet DHPTS01 must be turned on. **The LSP LINAC state is** therefore **mandatory when the AEX timing state is set**.

State Incompatibility: LTO, LSB, LBT, LAC, AMR.

7) ACCUMULATOR EXTRACTION & MAIN RINGS INJECTION (AMR).

The AMR state performs the same functions of the previously described AEX state enabling in addition the triggers for the injection into the Main Rings (kickers, diagnostics). **For the selection between Electron and Positron Main Rings the particle mode bit must be used**. **The Main Rings kicker power supplies need a pre-trigger that must be enabled by the VKP state** (see dedicated description) that **must precede AMR by exactly 7 states**.
It is worthwhile to remark that the same rules as for AEX case apply and in particular also **AMR needs to be preceded by the pre-triggers VM1 and VM2** and **two consecutive AMR states must be separated each other by at least 24 timing states**. Moreover, for the same reason, **24 timing states must separate the AEX state from the AMR (and vice versa)**.

State Incompatibility: LTO, LSB, LBT, LAC, AEX.

8) PULSED MAGNET DHPTT01 PRE-TRIGGER (VM1).

As already mentioned in the AEX and AMR states description, the VM1 gives a pre-trigger to the DHPTT01 power supply. This pre-trigger makes the power supply to invert the polarity for the Accumulator beam extraction. T**he VM1 state must precede the AEX or AMR states by exactly 5 states**, moreover the inversion phase takes ~ 95 ms, implying that, in order to prevent inadvertent passage of the beam inside the magnet during the inversion operation, the **VM1 state and the following 5 states are not compatible with LAC**.

State Incompatibility: LAC, AEX, AMR.

9) PULSED MAGNET DHPTT02 PRE-TRIGGER (VM2).

As already mentioned in the AEX and AMR states description, the VM2 gives a charging pre-trigger to the DHPTT02 power supply. T**he VM2 state must precede the AEX or AMR states by exactly 24 states**.

State Incompatibility: LAC, AEX, AMR.

10) PULSED MAGNET DHPTS01 PRE-TRIGGER (VMS).

As already mentioned in the LSP state description, the VMS gives a charging pre-trigger to the DHPTS01 power supply. **The VMS state must precede the LSP state by exactly 24 states**.

State Incompatibility: LAC, AEX, AMR.

11) MAIN RINGS KICKERS PRE-TRIGGER (VKP).

The VKP enables a charging pre-trigger to the Main Rings kickers power supplies. **The VKP state must precede the AMR state by exactly 8 states**. **For the selection between Electron and Positron Main Ring the particle mode bit must be used**.

State Incompatibility: AMR.

12) CALIBRATION STATE (VCA).

This timing state, compatible with all of the others, permits the triggering of any device in the absence of beam. This feature can be useful for calibration, frame subtraction, etc..

State Incompatibility: none.

3. Timing Dispatcher and Timing Receiver Module

The timing state word dispatcher module is performed by a VME slave board mapped in the A16/D16 space as two 16-bit registers [1]. This module distributes a new state word every 20 ms. A timing state word can be built up by one or more 16-bit words.

The timing dispatcher receives two 50 Hz square waves 90° apart from each other (ϕ_1 and ϕ_2) through two front panel BNC connectors. In this way it is possible to build a finite-state machine with four 5 ms states in the dispatcher module. After a constant delay from the beginning of the chosen state, the machine state word is broadcasted through a 4 twisted pairs RS485 serial link to the timing receivers located in the DAΦNE plant [2].

Timing precision in the machine state word distribution is limited by the following factors:

- 50 Hz phase jitter;
- dispatcher software uncertainty: ± 62.5 ns maximum;
- receiver software uncertainty: ± 25 ns maximum.

The dispatcher module broadcasts on the same RS 485 lines a 50 Hz sync signal that makes the timing receiver modules able to release the machine state word every 20 ms on the local bus. This is a dedicated bus using the a and c rows of the J2 VME connector, in a compatible way with VXI specifications [3].

In table 2 a list of timing state bits and pins.

Table 2. State bits and pins list

TOKEN	Table 2 - DAFNE Timing State Bits and Pins List DESCRIPTION	FAMILY	LOCAL BUS	J2 PIN
BE0	Bucket number enable 0	RF & Trigger	address 0	A26
reserved	Bucket number enable 1	RF & Trigger	address 1	C26
reserved	Bucket number enable 2	RF & Trigger	address 2	A27
BN0	Bucket number (1:120) / Least Significative Bit	RF & Trigger	address 3	A5
BN1	Bucket number (1:120)	RF & Trigger	address 4	A6
BN2	Bucket number (1:120)	RF & Trigger	address 5	A8
BN3	Bucket number (1:120)	RF & Trigger	address 6	A9
BN4	Bucket number (1:120)	RF & Trigger	address 7	A11
BN5	Bucket number (1:120)	RF & Trigger	address 8	A12
BN6	Bucket number (1:120) / Most Significative Bit	RF & Trigger	address 9	A14
reserved	-		address 10	A15
VCA	Various Calibration	Various	address 11	A17
VMS	Pulsed Magnet DHPTS01 Pre-trigger	Various	address 12	A18
VM1	Pulsed Magnet DHPTT01 Pre-trigger	Various	address 13	A20
VM2	Pulsed Magnet DHPTT02 Pre-Trigger	Various	address 14	A21
-	-	-	ibus clock	C27
LTO	LINAC Triggers OFF	LINAC	data 0	C5
LSB	LINAC Stand By	LINAC	data 1	C6
LSP	Beam from LINAC to Spectrometer	LINAC	data 2	C8
LBT	Beam from LINAC to BTF	LINAC	data 3	C9
LAC	Beam from LINAC to Accumulator Ring(Acc.Ring Injection)	LINAC	data 4	C11
VKP	Main rings kicker pre-trigger	Various	data 5	C12
e+	Particle mode: electrons(0) or positrons(1)		data 6	C14
reserved	-		data 7	C15
AEX	Accumulator Extraction	Accumulator Ring	data 8	C17
AMR	Accumulator Extraction & Main Rings Injection	Accumulator Ring	data 9	C18
reserved	-		data 10	C20
reserved	-		data 11	C21
reserved	-		data 12	A23
reserved	-		data 13	C23
reserved	From dispatcher to devil: 50Hz phase 2		data 14	A24
reserved	From disp.to devil: 50Hz ph.1/from receiver to devil: 50Hz SYNCH		data 15	C24

References

[1] A. Drago, *DAΦNE Timing System: State Word Dispatcher/Receiver*, CAS 94, Baden bei Wien, September 1994.

[2] A. Drago, G. Di Pirro, A. Ghigo, F. Sannibale, M. Serio, *The DAΦNE Timing System:*, EPAC 96, Sitges, June 10-14, 1996.

[3] *VXI Bus System Specification*, Revision 1.4, April 21, 1992.