DAΦNE TECHNICAL NOTE

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THOUGHTS ON POSSIBLE TRANSVERSE FEEDBACK SIGNAL PROCESSING SCHEMES FOR DAΦNE

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Introduction

The two-pickup processing scheme proposed for DAΦNE and PEP-II implements a quadrature phase shifter to compute any phase of correction signal from the input pick-up signals. The processing must be adjustable to allow for variations in betatron phase separation of the pickups due to tune changes, and the processing must provide a measure of DC orbit offset rejection to prevent saturation of the output stage. The processing scheme may also usefully incorporate diagnostic features, such as special features to allow tune measurement of a single uncontrolled bunch, special circuits to assist in adjusting the phase and magnitude of the correction signal, and special features to allow accelerator measurements (such as the measurement of instability growth rates). Our collaboration experience from the ALS suggests several potential schemes to implement for DAΦNE.

The transverse feedback systems in operation at the ALS are all analog systems, based on the two pickup quadrature scheme. The pick-up signals are detected at 3 GHz (the sixth harmonic of the ring RF) and processed in a two tap FIR filter constructed of a heilax cable delay line and hybrid junctions. In the front end detection circuitry a SUM signal at 3 GHz and an RF hybrid is used to achieve a modest degree of DC offset removal - the bulk of the DC removal is done with the two-tap FIR (which achieves around 20 dB of DC removal). In operation the ALS system required considerable time investment to optimally time the FIR delay line (which is a big spool of cable in a temperature stabilised enclosure). Adjusting the quadrature coefficients has been an iterative process, with a fair amount of manual "tweaking" from the operators for various observed instabilities on the beam.

In our original longitudinal design study, we thought it very difficult to implement a true multiplying FIR filter at the bunch crossing rate - and I think all would still agree. We went to the downsampled processing approach in the longitudinal systems for this reason. The KEK B factory two tap FIR processing approach is not downsampled, but is restricted to addition operations only and is still quite complex, with a 490 mm long motherboard populated with 16 daughterboards, external A/D and D/A cards, etc.

A Novel Hybrid Multiply/Accumulate Circuit

One idea that looks very interesting is to use digital components to implement the sampling and delay functions of the processing but use analog circuits to implement the multiply/accumulate functions of the feedback filter. This hybrid approach would allow the construction of FIR and IIR filters at the full bunch crossing rate, and allow inclusion of a sub-set of the diagnostic/machine physics functions in the digital portions of the system.

Our experience with the longitudinal systems using digital processing techniques suggests that a hybrid analog/digital processing scheme could be constructed for DAΦNE that would likely be useful for a wide variety of machines (including PEP-II, ESRF, KEK B factory, etc.).

The essential functional blocks of this hybrid scheme are sketched in Fig. 1. We would anticipate using front end processing techniques in the manner of the ALS systems, and for each set of pick-up buttons a receiver would detect at some selected RF frequency, and produce a baseband signal for X and Y positions at that receiver. The baseband beam motion output would be sampled by a high speed A/D converter at the bunch crossing rate. I think it necessary to incorporate a significant degree of orbit offset removal in this processing block to preserve the limited dynamic range of the subsequent digital processing. The simplest candidate technique would be to use information from the digital data stream at a downsampled rate, averaged to compute a DC component which a low frequency feedback loop would remove via a correction signal added to the baseband stream. The downsampled stream could be from a single selected pilot bunch, or a slow sampling of all the populated bunches. The baseband stream would still contain a small DC orbit component, largely due to the variations in current of each bunch. The residual DC offset components would be removed in the subsequent FIR processing blocks.

The digital data stream now contains bunch by bunch transverse position information. This data stream would be processed in a memory structure very much like the longitudinal systems' hold buffer - a fast memory which allows interleaved writes and reads using two independent memory pointers. An autoincrementing write pointer writes the input data into the buffer, while the autoincrementing read pointer reads data from the memory and passes it to the output D/A stage. Maintaining an offset between the write and read pointers implements a time delay in the data stream, adjustable to obtain one turn or fractional turn delays.

The multiply function of the FIR-IIR convolution filter can be constructed in a hybrid fashion by using fast D/A converters at the output of the hold buffer with multipliers (bipolar attenuators or mixers) in the analog output. The tap weights (coefficients of the filter) are programmable in this scheme, but are common to all bunches. The accumulate function is implemented in a wideband resistive summing circuit which adds the outputs from a number of multiplying tap stages. The number of summed signals determines the order of the filter, while the topology of the summing allows either FIR or IIR filters to be constructed.

The two tap FIR filter requires a tap separation of exactly one turn, while the cable delays and propagation delays in the system require an additional delay to allow the computed kick signal to arrive at the kicker at the proper time to influence the correct bunch. For small rings this time delay can be implemented as delay cables - for a more general purpose delay adjustment I think the hold buffer function should be structured as shown in Fig. 2, where the two taps of the filter have independent read pointers, allowing a time offset between input and output while maintaining a consistent one-turn delay between the two filter taps.

The one-pickup one-plane processing block would be composed of a VXI processing module, containing a complete receiver, DC offset removal circuit, A/D circuit, two output hold buffer with two D/A outputs, two bipolar mixer/multipliers, and two low-speed D/A circuits to implement the tap coefficients under program control.

A two-pickup processing channel would be composed of two VXI modules, with a four-input wideband summing node to generate the correction kick signal. Also note the general flexibility in this processing module - a 4 tap filter could be composed of 2 such modules, etc. This central building block could serve as the heart of quite a variety of filter/processing functions.

To stimulate discussion, here are a few comments on the challenges I can see in each function block, and a few comments on possible implementations.

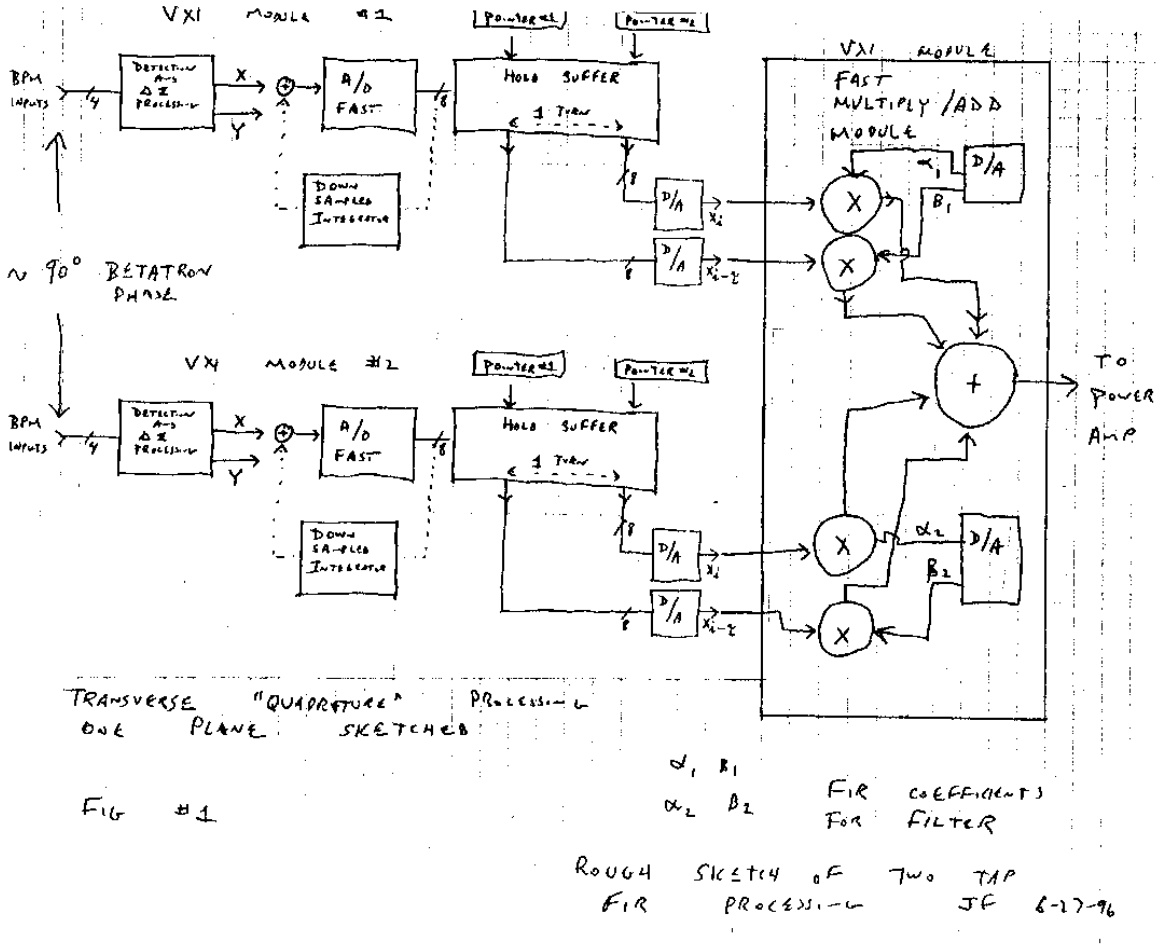

Figure 1 – Two Tap Hybrid FIR Processing Scheme.

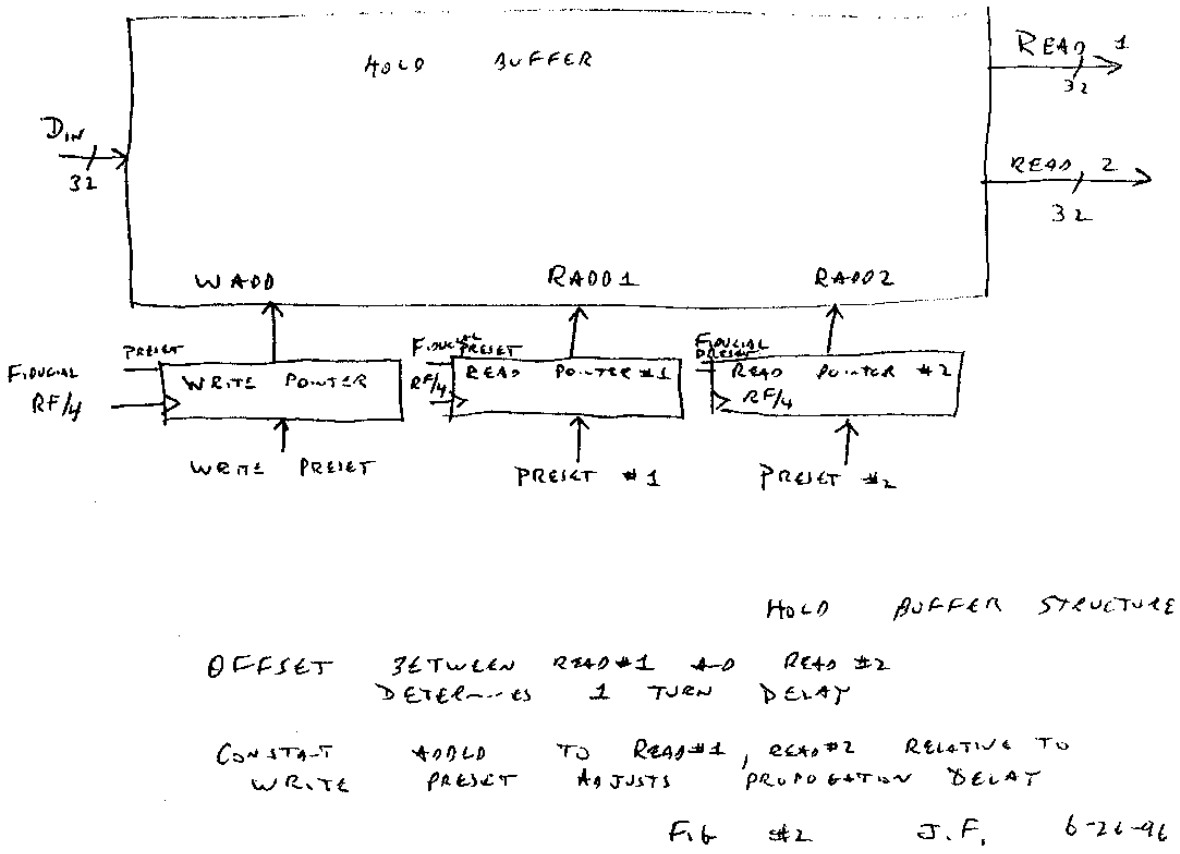

Figure 2 – Hold Buffer Structure

Front End Receivers

Here the difficulty is in the proper matching/calibration of the 4 button channels, and the technique selected to compute the beam centroid. Given our wideband system, I think synchronous detection at some harmonic of the RF (RF*3, RF*4, etc. depending on the propagation cut-off of the vacuum chamber) followed by passive sum/difference hybrids (the monopulse comparator scheme) seems the way to go. Walt Barry has explored homodyne as well as heterodyne detection, and here I think a choice is not clear.

DC offset removal circuitry (front end)

To attempt to preserve as much dynamic range as possible I suggest doing a reasonable amount of offset rejection in the front end, followed by the DC rejection in the FIR filter structure. I would down-sample the fast A/D stream and add a slowly varying DC offset correction to the beam motion as sketched in Fig. 3. The simplest approach to computing this feedback offset correction is to always sample a single pilot bunch (a known filled bucket) but a more sophisticated approach would pick out a selected bucket on a given turn, and then pick out another bucket on a later turn, and sample a table of filled buckets over time, eventually returning to the first sampled bucket . I think there is not much offset removal advantage to the fancier approach, but the flexibility of the table driven sampler appeals to me. I would suggest implementing the fast latch and sample selector using the logic currently used in the longitudinal downsampler for the exception bucket logic, and latch the selected sample on the bucket count match. The integrator/filter in this scheme would be easily implemented in a DSP chip such as the AT&T 1610 - which would drive an output slow D/A to generate the DC offset injection circuit. Note that the 1610 could easily implement a sampling table and load the bucket selection logic from some sampling pattern or table. There is also a very useful diagnostic function possible here, in that the 1610 can therefore sample any bunch for N turns and keep the values in memory, or do a variety of DC calibrations of the front end and A/D circuits.

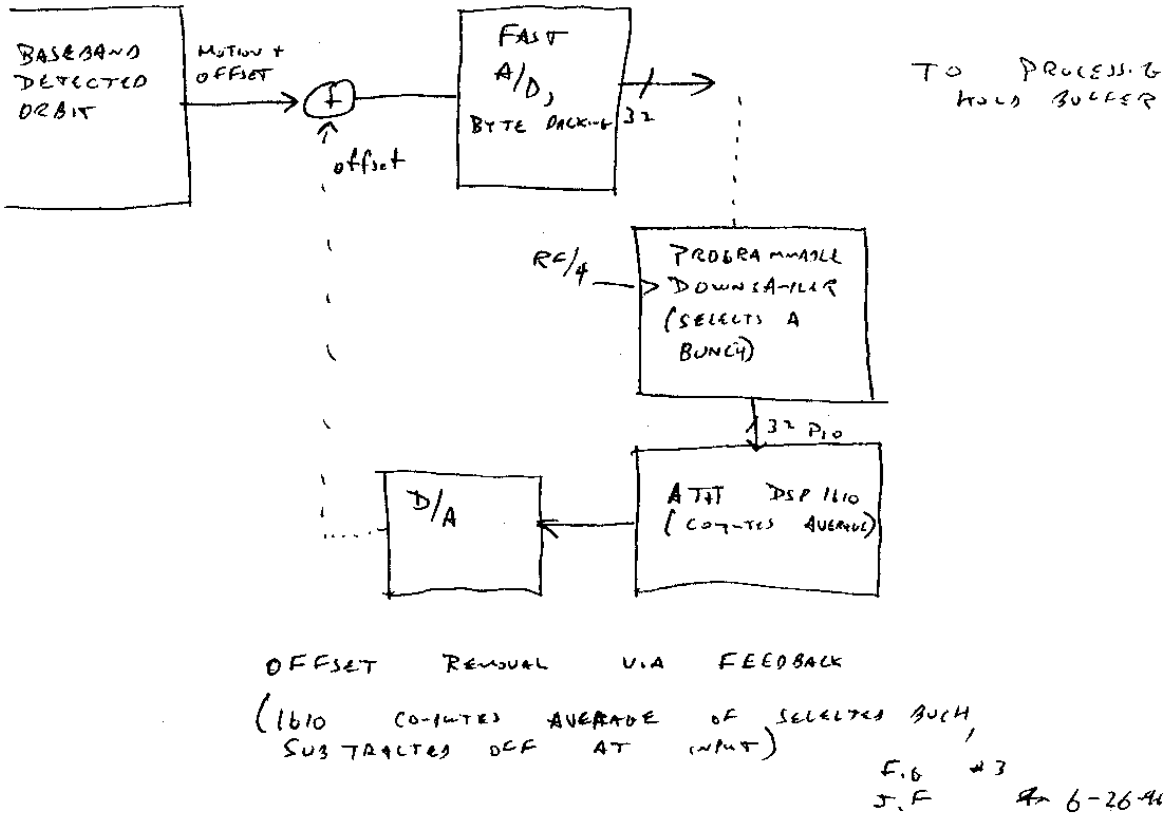

Figure 3 – Front End Offset Rejection.

A/D circuitry

I would use exactly the front ends and 500 MHz digitizers of the existing systems, building on our parts inventory and design expertise.

Hold Buffer Memory and D/A outputs

Here our design experience with the longitudinal systems is directly relevant. I would suggest using the same group-of-four processing block as implemented in the longitudinal systems, in which four consecutive samples are concatenated to create a 32 bit word. The interleaved write/read cycles therefore occur at a memory cycle time of two bunch crossings - 4 ns for the 500 MHz systems. Our experience with the selected fast ECL memories in the longitudinal downsamplers prove this approach - the rings with lower RF frequencies or lower sampling rates use slightly slower memory cycles.

Of course, this group-of-four processing requires either that the ring harmonic number by divisible by four, or that the remainder bunches are not processed and need to be in a an empty gap.

This is not a problem for DAΦNE or PEP-II, but we should check on the ESRF and Synchrotron Trieste cases.

A very real concern in this block is the availability of the fast ECL memory. We have a limited stock on hand of the selected 4 ns memories, plus a larger inventory of the standard 5 ns parts (which would support 400 MHz sampling rates in this scheme). Availability of either part looks poor in the future. Easily available memories seem to have 12 - 15 ns cycle times, which would require use of a group-of-eight approach, greater restrictions on the harmonic number/gap issue, and double the number of parts in the hold buffer memories. Personally, I would try to buy up the last available parts of the 5 ns memory and use exactly the circuits from the longitudinal systems.

D/A stages

I would use the fast Triquint part we are using for the longitudinal systems - with the current output it is perfect for the planned application. The multiply operation requires a double balanced mixer - I think our bandwidth (which goes down to near DC and up to several hundred MHz) could be achieved with an active Gilbert-cell multiplier. Alternatively, it may be possible to use passive approaches though I cannot see any advantage to the passive components. I would set the tap coefficients from a low-speed D/A circuit, so that the coefficients were digital numbers loaded via the VXI/VME backplane. I think the proper place to build these multiplier/accumulator circuits is in the summing node/output stage module.

Summing nodes

I would develop a fast DC coupled n input summing stage, either with passive summers or active DC coupled circuits from Comlinear (we would want something like 400 - 500 MHz bandwidth, consistent with not degrading the power amplifier bandwidth). I would put here the N active multipliers and N DAC channels of coefficients. In this module I would also include overall gain control circuits to scale the output to the proper levels for the power amp inputs. I would also implement a fast output modulator to allow turning on/off the output for grow-damp measurements, or inverting the output signal phase.

Diagnostic functions

It would be very desirable to include a means of turning off the feedback for a single selected bunch to allow a tune measurement. With this architecture we can use the downsampled data stream for a selected bunch, and pass this stream through the DSP, and directly compute the tune in the DSP (the DSP would be fast enough to sample a single selected bunch for a record of several thousand turns, then return to calculating the slowly varying DC offset correction). While the tune measurement is in progress the data for the selected bunch could be forced to a full-scale value or zero, effectively disabling the feedback of a selected bunch. This would also allow an external measurement of the tune to be made via an excitation of the beam and measure of the response via traditional lab instruments.

Another useful diagnostic function would be a means of adjusting the quadrature coefficients via the use of the two pickup signals and a signal induced by the beam in the kicker. As suggested by Mario Serio, the basic idea is to use the beam induced kicker signal as a phase reference and automatically adjust the quadrature coefficients to enforce a 90 degree phase shift between combined pickup signals and the kicker. There is a calibration procedure to work out to account for the propagation delays between the processing chassis and the kicker, but the necessary circuit functions could be incorporated as part of the system design.

Finally, it would seem useful to include a fast multi-bunch memory to allow grow-damp and growth rate measurements. If the growth rates are in the millisecond range, the memory should span possible record intervals of up to 10 or 20 ms. If the data is written for every bunch on every turn, the total memory size required for the DAΦNE machine would be something like 32K samples per bunch, or around 3.5 Msamples total. This would be a messy amount of fast memory to include, given the modest density of the fast ECL memory (2k or 4k bytes/chip). However, if the purpose of the memory record is to measure growth rates and infer modes from the bunch motion, it is adequate to record the bunch motion at a downsampled rate. This approach would allow the measurement of the relative phases of the individual bunches, as well as the amplitudes of the envelope of motion of each bunch - even though the measurement would be at an aliased frequency determined by the effective sampling rate and the machine tune. Because the actual machine tune is known/measured, it is possible in a post-processing program to completely recovered the un-aliased bunch motion if desired.

The available dense memory (in 128Kbyte sizes) has cycle times in the 20 ns range, so that a complete DAΦNE 10 ms time record can be fit into 4 memory packages using a downsampling factor of 8 (or 20 ms using a downsampling factor of 16). I would expect that our experience with the longitudinal systems should allow us to make a very compact table-driven downsampler and record memory, useful for performing grow-damp dynamic measurements.

In summary, I think the transverse feedback processing functions and several very useful diagnostic functions could be designed into a general-purpose VXI module, and a complete plane of processing for a two pickup system implemented using two such processing modules and a summing/output stage module. This approach would be very general-purpose and useful at a variety of laboratories. I hope that we can collaborate on these ideas and potentially construct a family of transverse processing modules for DAΦNE.

Acknowledgments

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